Parameter analysis and optimization of phase interpolators of different architectures in low-scalable CMOS technology (2023)

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***Abstract*—This document provides a description of two different architectures of Phase Interpolators (PI) that are used in clock and data recovery systems. Both PI blocks have been implemented in 16 nm technology using same 0.9V power supply. Despite the discrepancies in pinout, testbenches used to compare architectures have been prepared to ensure similar operating conditions of the system. The research assumes that the bitrate is equal to 9 Gb/s and there are four input clocks shifted in phase by 45° in reference to the previous one. The number of interpolation steps is 64 per bit duration (UI). Comparison refers to the most significant parameters with focus on DNL (*Differential nonlinearity*), INL (*Integral nonlinearity*), power consumption and layout area.**

***Index Terms*— CMOS, PLL, DLL, CML, DNL, INL, ADC, UI, Phase Interpolator (PI), multi-step, cascade PI.**

I. INTRODUCTION

The Phase Interpolator is a crucial element in the complex process of receiving data in various data interfaces like USB, HDMI, DDR, MIPI. The circuit allows to adjust the phase of the sampling clock in fine steps.[1] It provides the opportunity to support multiple standards, bitrates and to increase the flexibility of the entire system.[2] Mostly PI is applied in high-speed circuits like delay locked loop (DLL) or phase locked loop (PLL).[3]

With the technological development and minimization of dimensions, engineers try to optimize the area of the systems, power consumption and reach desired data rates. The system functionality could be the same, but the architecture can be considerably different. This paper reports the results of research regarding the differences between CML and cascade architecture of a Phase Interpolator.

II. PHASE INTERPOLATOR

The main purpose of an analog phase interpolator is to create a specified phase of the clock in relation to reference clock. The equation describing the correlation between the output clock and input signals is presented below [4]:

$$\varphi_{01} = \left(\frac{n}{N}\right)\varphi_1 + [(N-n)/N]\varphi_0$$

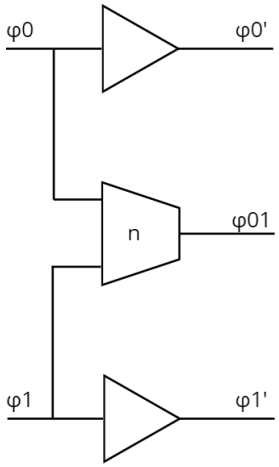

Fig. 1 Basic concept.

where:

- φ_{01} – output signal
- φ_1, φ_0 – input signals with different phase with and assumption that $\varphi_1 > \varphi_0$.
- n – defines the specific phase step number ∈ <0:N>,
- N – total phase step,

The control of PI can be implemented in many ways, but the base concept assumes usage of the weighting factor n. The weighting signal is transformed into the appropriate value of phase shift (Fig. 1).[5]

The input signals should have the same shapes, be periodic, overlapped and phase spacing needs to be constant. [2,5]

III. PARAMETERS OF PI

The main parameters characterizing the phase interpolator are DNL (Differential nonlinearity) and INL (Integral nonlinearity).

DNL (Fig. 2) is an error that describes the difference between the ideal value of 1LSB and the measured step. The ideal analog-to-digital converter (ADC) should provide a DNL value equal to 0 LSB for every step. The specification for this parameter is 1LSB because it assures the monotonic function of transmission without missing codes.[6]

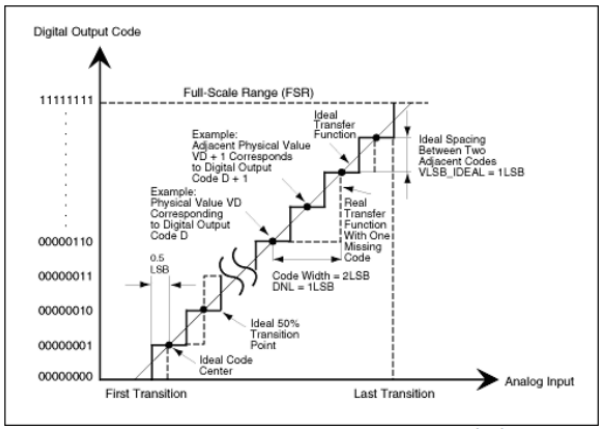

Fig. 2 DNL visualization.

INL is a deviation of the real signal from a straight line representing ideal circuit. As mentioned in [7] the mixing ratio can be linear, trigonometric, and non-linear to accomplish the highest linearity of the output signal of Phase Interpolator. (Fig. 3).

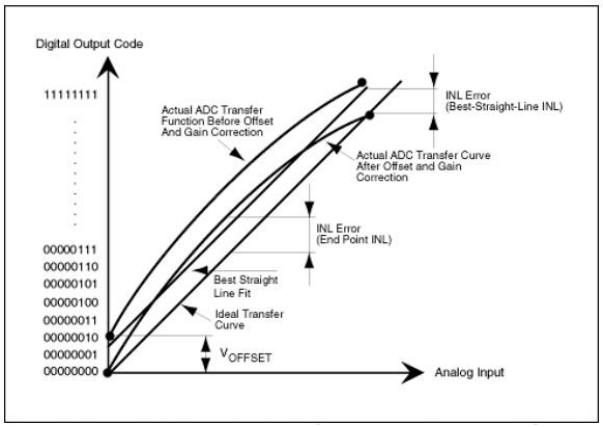

Fig. 3 INL visualization.

The correlation among INL and DNL is represented by below function [8]:

$$INL(n) = \sum_{i=0}^{n} DNL(i)$$

III. CML ARCHITECTURE

The current-mode logic architecture of PI is based on classic differential pair design with a symmetric resistive load which interpolates two nearest given phases [5].

Phases are interpolated accordingly to given weights which come from the DAC R2R ladder. Input 7-bit code is converted to a specific voltage value which varies from 0V to a power supply voltage. The signal from the R2R ladder is applied to the selection input of PI to turn on differential pair transistors, which in this architecture are acting also as current limiters.

The block diagram of current-mode logic of PI is presented in Figure 4.

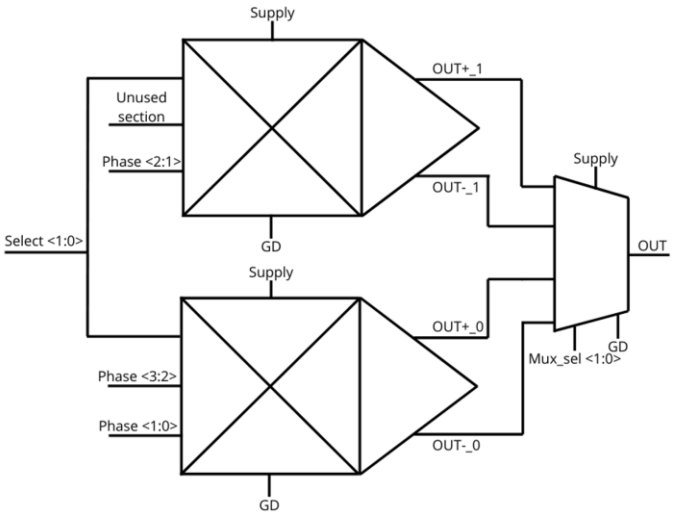

Fig. 4 Block diagram of CML PI.

While interpolating two given phases (φ0 and φ1), with equal select code for both inputs, the output voltage should be in the middle of φ0 and φ1. While setting φ0 input to a higher voltage (code), the output phase should be closer to φ0. Figure 5 represents the input stage of the unit cell of the designed PI. Respectively, applying more voltage to φ1 than φ0 select input will force the output phase to be closer to the φ1.[5]

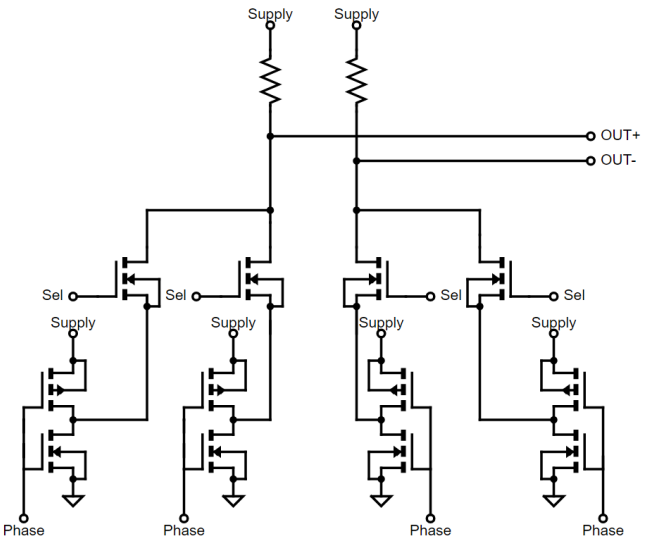

Fig. 5 Input stage of the unit cell of the CML PI.

It is not possible to use every code from the R2R ladder to interpolate given clock phases. Respectively, the lowest and highest codes are undesirable since transistor's characteristics are non-linear. The input voltage must be slightly higher than the threshold voltage of a single device to make it operating in sub-threshold region and highest gm. The voltage must not be too high since the output voltage ought to have a wide swing. It is crucial to select proper codes for the designed W/L ratio of the transistor to interpolate phases properly what is ensured by special bias circuit.

IV. CASCADE ARCHITECTURE

The concept of the following architecture is significantly different from the conventional PI. Due to voltage limits and power consumption, architecture is based on inverters and simple logic gates that can ensure significantly better performance. It is important that the power consumption increases when there is a need for high resolution or a wide range of frequencies.

Thanks to the multiple steps of cascade, it is possible to implement any number of interpolation steps just by adding 1-bit cells in series. As mentioned in [3] resolution like that can considerably reduce the layout area of the PI. To achieve 8 steps of interpolation it is required to use 3 instances. The block diagram of the system is presented in Figure 6.

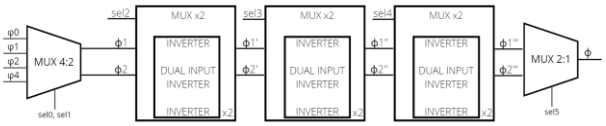

Fig. 6 The simplified architecture of cascade phase interpolator.

The phase selection is performed through the MUX located at the input of the circuit. The 2-bit word is obligatory to control the choice of an appropriate phase to mix. The most efficient operation of the system provides a difference of phases of no more than 45°. In every cell, there are also 2 inverters (at the input and the output) to improve the sharpness of the signal for the next stage. There is also a reference path to replicate the original phase to eliminate the differences in the propagation time of reference signal for the next stage. That is why there are additional MUX cells. (Fig. 6) The output signal is selected by one more MUX at the output of the circuit.

The core of the circuit is the inverter biased with specific current value. The biassing technique is a current mirror and the value of the current is defined by a weighting factor.(Fig.7)

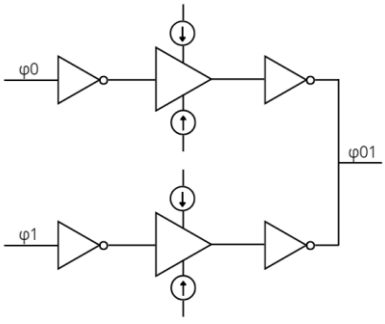

Fig. 7 The concept of the core.

The phase of the resultant signal should be in the middle of φ0 and φ1 (Fig. 8) The relation between slew rate and delay of two input signals is crucial. It is important to control this ratio – rise time [3]. If the difference is not respectively maintained the output level is undetermined.

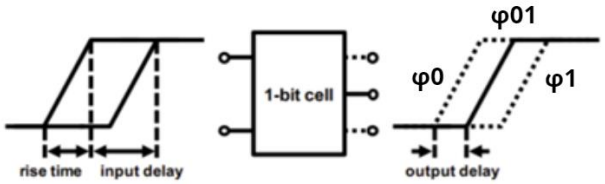

Fig. 8 Principal of operation for 1-bit cell.

V. PROJECT ASSUMPTIONS

The study assumes four input clocks from a ideal VCO (Voltage Controlled Oscillator) which are shifted in phase by 45° resulting in having 0°, 45°, 90°, and 135° reference phases. The next design assumption is dividing the UI (360°) into 64 steps. This means that between every input clock there should be 8 steps equal to 5.625° per each.(Fig. 8).

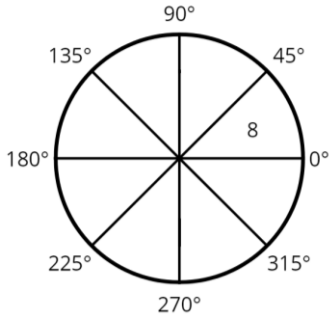

Fig. 8 Division of steps.

VI. SIMULATION RESULTS

VI.I. CML ARCHITECTURE

The CML architecture results have proven that the design works properly.

The results for the DNL are in range 0.006-0.206 LSB. Figure 14 presents the DNL/INL plots for CML architecture.

The estimated area of the CML architecture is significantly larger than the area of the cascade architecture (Fig. 15). It is caused by the output stage of the unit cell of the PI, which consists of two inverters (one for OUT+ and one for OUT-). The inverters work as linear amplifiers, and the area of linearizing resistors (used in a feedback loop) is almost 80% of the area of the whole CML architecture.

The estimated area was calculated without including routing paths and with optimization of the current architecture. The optimization assumes applying only one unit cell of the PI instead of two (Fig. 4). The optimization can be done by multiplexing four input clocks into two and adding a new selection pinout. It leads to a change in the architecture of the output stage MUX. As a result, the output MUX would multiplex only two output clocks from the single unit cell of the PI instead of multiplexing four output clocks. (Fig. 4). The schematic design of an optimized architecture is shown in Figure 9.

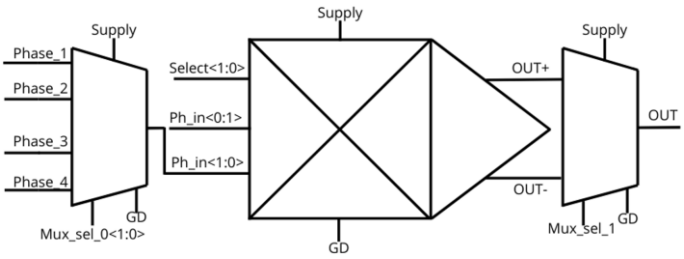

Fig. 9 Optimized architecture of CML PI.

Power consumption is equal to 3.38 mW but it also can be reduced during layout optimization.

Figure 10 shows the real phase shift for all 8 regions between the two nearest input phases. Respectively, the average mismatch between the real-shifted and ideal-shifted phase is 0.223° which corresponds to an average mismatch of 0.134 ps.

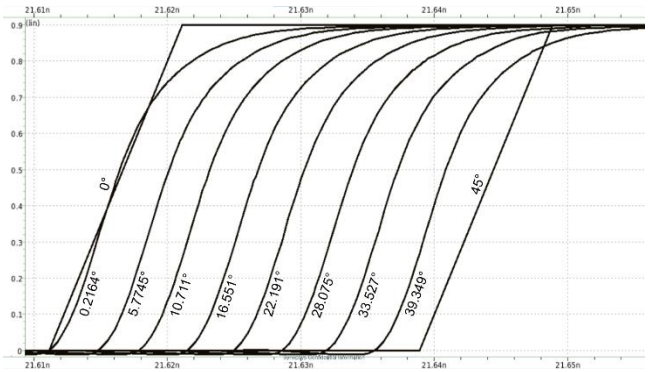

Fig. 10 8-step interpolation between two phases.

Figure 11 shows the correlation between two select input voltages for all interpolation steps.

The summary of results is presented in Figure 15.

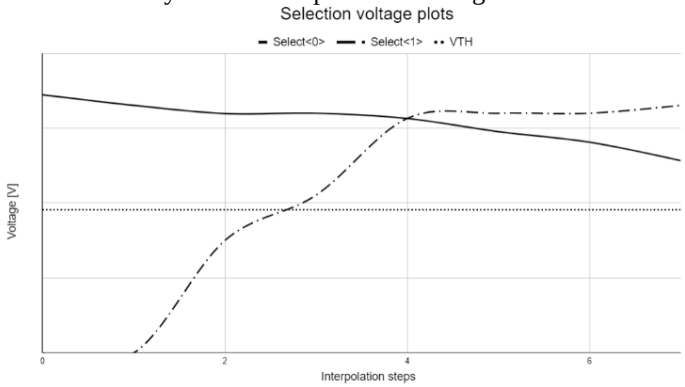

Fig. 11 The relation between select input voltages.

VI.II. CASCADE ARCHITECTURE

The cascade architecture fulfils the established functional requirements of the phase interpolator. Figure 12 represents the correlation of next interpolated phases. The average error of phase shift is 0.664°.

The range of DNL is 0.092-0.417 LSB. It means no codes are being missed. Figure 14 presents the DNL/INL plots for architecture.

The architecture mainly consists of inverters, so the estimated area (without routing paths) is small - 5.345 μm².

The power consumption is high because of the output inverters of every core cell is connected to a short circuit net.

Every stage of the phase interpolator increments the error of the duty cycle, especially the last one. Thanks to the use of multiple inverters the rise/fall time of the signal is relatively small in comparison to the input one. Unfortunately, there is a mismatch between these values.

The summary of results is presented in Figure 15.

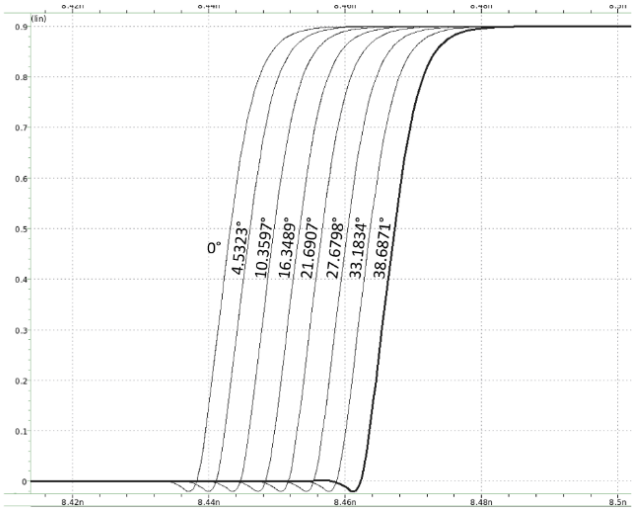

Fig. 12 8-step interpolation between two phases.

To achieve full range of work it is obligatory to change MUX settings. Two MSB are responsible to choose the appropriate input phase to interpolate (2b'00 - 0°/45°; 2b'01 - 45°/90°; 2b'10 - 90°/135°). Figure 13 describes the correlation of setting pins and the output phase in selected range . The three ones select the relevant value for the reference path. The last is connected with the choice of output signal – from reference path or interpolated one.

Select signal <3:0>	Output phase [°]
4b'0001	0
4b'0000	+5.625
4b'0011	+11.25
4b'0110	+16.875
4b'0101	+22.5
4b'1100	+28.125
4b'1111	+33.25
4b'1010	+39.875

Fig. 13 Control pin settings.

VI. SUMMARY

The result of the research work compares two significantly different phase interpolator architectures.

The control of both architectures assumes a similar number of bits but the CML one requires DAC to provide full functionality. The cascade architecture is characterized by shorter rise and fall time. However, the duty cycle of the output signal is not an advantage. The CML architecture provides correct performance in this aspect. The results of DNL/INL for the cascade solution are inferior to the second one because of the wide range of interpolation. (Fig.14)

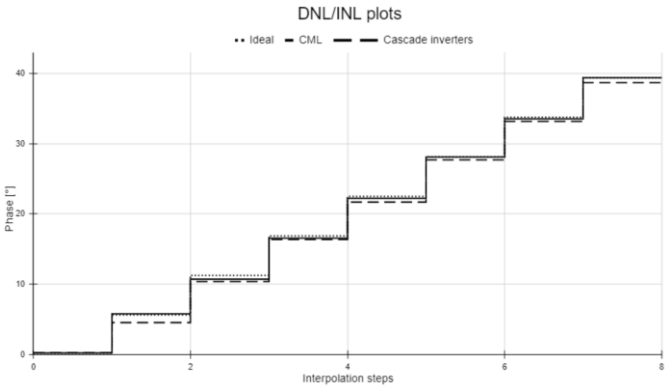

Fig. 14 Comparison of DNL/INL parameter.

The power consumption of both circuits is high but the CML one's is reduced by half. On the other hand, the estimated layout area is significantly lower for the second circuit. The comparison of most significant parameters is shown in Figure 15.

Both architectures have the same functionality but are used in different implementations of circuit design.

Parameter	Unit	CML	Cascade
Averaged DNL	[LSB]	0.0829	0.2511
Averaged error of phase shift	[°/ps]	0.223/0.134	0.664/0.406
Output rise and fall time	[ps]	9.47/9.04	8.26/7.47
Output duty cycle	[%]	49.41-50.66	58.51-59.49
Power consumption	[mW]	3.38	6.06
Estimated area*	[μm²]	13.823	5.345

*Area without routing paths. For CML estimated area after optimization and without R2R DAC.

Fig. 15 Comparison of architectures.

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